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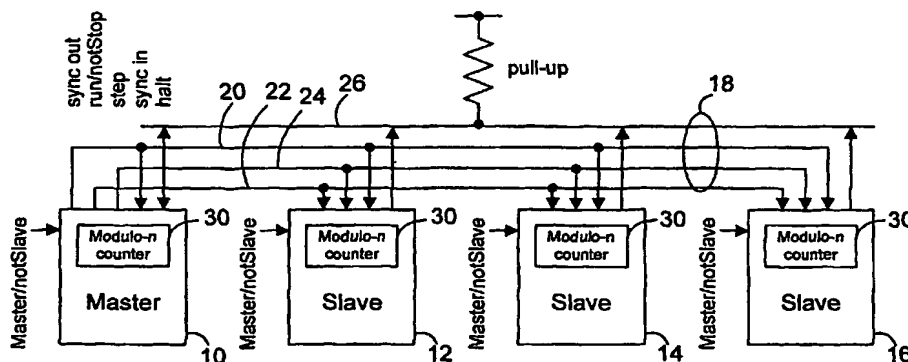
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ning of each regular issue of the PCT Gazette.*

(54) Title: ARRAY SYNCHRONISATION



(57) Abstract: A method is disclosed for achieving synchronization in an array of semi-synchronous devices. A processor array has an array of processor elements, wherein each of said processor elements comprises a cycle counter, and a master processor element is able to transmit control command signals to each of the other processor elements. Each processor element is such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and the master processor element is such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range, or "safe window". By appropriate setting of the "safe window", it can be guaranteed that, when the master processor element transmits a control command signal to each of the other processor elements, those command control signals are acted upon at corresponding times within the other processor elements.

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F15/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GREENSTREET M R: "Implementing a STARI chip" COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, 1995. ICCD '95. PROCEEDINGS., 1995 IEEE INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA 2-4 OCT. 1995, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 2 October 1995 (1995-10-02), pages 38-43, XP010197289 ISBN: 0-8186-7165-3 page 38, left-hand column - page 39, right-hand column; figure 1	1-10
A	US 6 055 285 A (ALSTON JERALD) 25 April 2000 (2000-04-25) columns 5-8 ----- -/--	1



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>WO 02/50700 A (CLAYDON ANTHONY PETER JOHN ; PICOCHIP DESIGNS LTD (GB)) 27 June 2002 (2002-06-27) page 11 pages 17-19; figure 1 -----</p>	1

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			AU 9576801 A	01-07-2002
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